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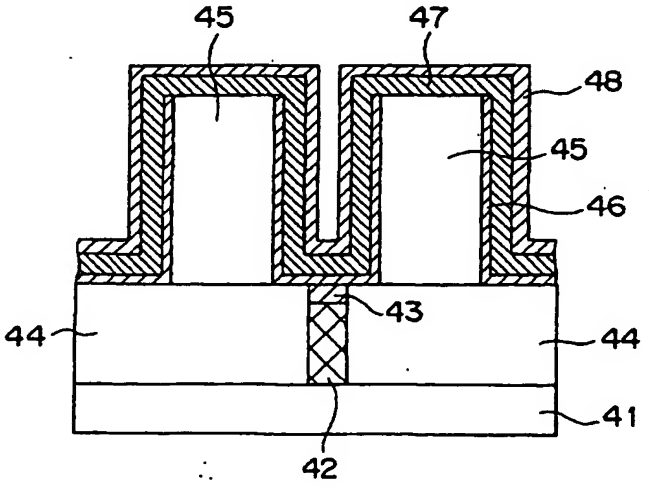
(54) SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

(57) A semiconductor device containing a dielectric capacitor having an excellent step coverage for a device structure of high aspect ratio corresponding to high integration degree, as well as a manufacturing method therefor are provided. A dielectric capacitor of high integration degree is manufactured by forming a bottom electrode 46 and a top electrode 48 comprising a homogeneous thin Ru film with 100% step coverage while putting a dielectric 47 therebetween on substrates 44, 45 having a three-dimensional structure with an aspect ratio of 3 or more by a MOCVD process using a cyclopentadienyl complex within a temperature range from 180°C or higher to 250°C or lower.

FIG. 4



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Description

Technical Field

[0001] This invention relates to a semiconductor device containing a dielectric capacitor and a manufacturing method thereof and, more in particular, it relates to a semiconductor device in which an electrode comprising Ru, RuO_2 or a mixed material of Ru and RuO_2 is deposited homogeneously on a substrate with a three-dimensional structure and a manufacturing method thereof.

Background Art

[0002] Semiconductor memories include DRAM (Dynamic Random Access Memory) having a feature in high speed data rewriting. Along with progress in ultra large scaling integration technology, DRAM has entered a large capacitance of 256 M, 1 G bit. Therefore, integration has been demanded for circuits and, particularly, size of capacitors for storing information has been made finer. Means for the integration of capacitors can include reduction of film thickness of dielectrics, selection of materials of high dielectric constant and a three-dimensional structure comprising top and bottom electrodes and a dielectric.

[0003] Among them, for the dielectric material, it has been known that BST having a single unit cell of perovskite structure ($(Ba/Sr)TiO_3$) as the crystal structure has higher dielectric constant (ε)compared with SiO_2/Si_3N_4. An example of using high dielectric materials has been reported in Japan Journal of Applied Physics, 1995, 5077p (Jpn. J. Appl. Phys., 34, 5077, 1995). According to this report, since the condition for the aspect ratio (contact hole patterns of 800nm depth/240nm diameter) of the three-dimensional structure using BST is about 0.65, top and bottom electrodes and a dielectric are prepared by a sputtering method.

Disclosure of Invention

[0004] In the prior art described above, since Pt or Ru of the bottom electrode is prepared by the sputtering method, it involves a problem that the three-dimensional structure shows poor step coverage and adhesion to the inside wall is small compared with that to the surface and the bottom, so that a highly three-dimensional device structure with an aspect ratio of 1 or more can not be attained.

[0005] This invention has been accomplished to overcome the foregoing problems and intends to provide a semiconductor device including a dielectric capacitor having excellent step coverage in a device structure at high aspect ratio along with the trend of high integration degree, as well as a manufacturing method thereof.

[0006] Heretofore, although there has been a report of preparing electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 thin films by a sputtering method on a three-dimensional structure with a small aspect ratio, but a film forming technique by an metalorganic chemical vapor deposition process (MOCVD) has not been taken into consideration.

[0007] The present inventors have found that a homogeneous electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 thin films can be prepared on substrate having a three-dimensional structure within a temperature range from 180°C or higher to 250°C or lower by an MOCVD process using a cyclopentadienyl complex. The principle capable of preparing a homogeneous film in the temperature range described above is to be explained below.

[0008] Fig. 5 shows a crystal structure of a ruthenium cyclopentadienyl complex used in this invention. δ or π bonds are present between a 5 cyclic and ruthenium metal, and a temperature at 180°C or higher is necessary as the energy of dissociation in view of bonding energy. Further, the adhesion rate of the complex is constant on Si substrate within a temperature range from 180°C or higher and 250°C or lower and decomposition - adhesion on the surface proceeds preferentially at a higher temperature.

[0009] Accordingly, a film is formed only on the surface (top plane of protruded portions) in a substrate having a three-dimensional structure to form inhomogeneous films with the film thickness reduced on the inside wall and the bottom (top plane of convex portions). Particularly at a temperature higher than 300°C, island crystals are formed due to rapid decomposing reaction to form rough film quality for which contact can not be attained. Accordingly, a homogeneous electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 thin films can be formed to the surface, the bottom and the inside wall on a substrate having a three-dimensional structure by the MOCVD process using a ruthenium cyclopentadienyl complex within a temperature range from 180°C or higher to 250°C or lower.

[0010] Further, the present inventors have found that a electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 thin films can be formed homogeneously by the MOCVD process using a β-diketone complex within a temperature range from 300°C or higher to 500°C or lower when a structure having a three-dimensional is constituted of two insulation layers, namely, a surface layer with small adhesion rate and a inside wall layer with large adhesion rate. The principle is to be explained below.

[0011] Fig. 2 shows a crystal structure of a ruthenium β-diketone complex used in this invention. π bonds are present between oxygen in a 6 cyclic and ruthenium metal and can dissociate at a temperature of 300°C or higher in view of the bond energy. However, since dissociation of oxygen - carbon bond or dissociation of oxygen - ruthenium bond proceeds simultaneously, the adhesion rate is small and decomposition - deposition near the surface proceeds preferentially. Further, at a tem-

perature higher than 500°C, island crystals are formed due to violent decomposing reaction to result in film quality not capable of attaining contact. Then, as shown in Fig. 3, a homogeneous electrode thin film comprising Ru, RuO_2 or a mixture of Ru and RuO_2 can be prepared to the surface, the bottom and the inside wall within a temperature range from 300°C or higher to 500°C or lower by an MOCVD process using a ruthenium β-diketone complex on structure having a three-dimensional by constituting the structure having a three-dimensional with an insulation layer of a dual layered structure comprising a surface layer 31 having a small adhesion rate and a side wall layer 32 having a large adhesion rate, for example, MgO/SiO_2 or Al_2O_3/SiO_2 for the electrode material.

[0012] This invention has been accomplished based on the studies as described above, and it has a feature in a method of manufacturing a semiconductor device of laminating to form a bottom electrode, a dielectric and a top electrode on a substrate having a three-dimensional structure, wherein a bottom electrode and a top electrode are formed by a metalorganic chemical vapor deposition method at a temperature of 180°C or higher and 250°C or lower using a cyclopentadienyl complex as precursor.

[0013] The cyclopentadienyl complex is used as an Ru precursor and, particularly, dicyclopentadienyl ruthenium is preferred. The bottom electrode and the top electrode are formed each as a thin film comprising Ru, RuO_2 or mixture of Ru and RuO_2.

[0014] By using one of O_2, H_2, N_2O, O_3, CO and CO_2 as a reaction gas, decomposing reaction from the precursor can be promoted to form a film at a low temperature of 180°C or higher to 250°C or lower. Particularly, in a gas mixture of a reaction gas and a carrier gas (Ar, He or N_2 gas), the ratio of the reaction gas to the carrier gas is preferably 1% or more.

[0015] According to this feature, an electrode thin film can be prepared homogeneously to the surface, the bottom and the side wall on the substrate having a three-dimensional structure. Accordingly, it is possible to obtain a dielectric capacitor of high integration degree comprising a top electrode/a dielectric/a bottom electrode having a three-dimensional structure of high aspect ratio of 3 or more (contact hole depth/diameter).

[0016] Further, this invention has a feature in a method of manufacturing a semiconductor device of laminating to form a bottom electrode, a dielectric and a top electrode on a substrate having a three-dimensional structure, wherein the structure having a three-dimensional constituted of an insulation film of a two-layered structure comprising a surface layer with a small adhesion rate and a side wall layer with a large adhesion rate for the starting electrode material and the bottom electrode and the top electrode are formed by metalorganic chemical vapor deposition process using a β-diketone complex as the precursor at a temperature of 300°C or higher and 500°C or lower.

[0017] The β-diketone complex is used as the precursor for Ru and dibivaloylmethanate ruthenium is particularly preferred. The bottom electrode and the top electrode are formed each as a thin film comprising Ru, RuO_2, or a mixture of Ru and RuO_2.

[0018] A decomposing reaction is promoted at a temperature of 300°C or higher to 500°C or less to prepare a homogeneous electrode thin film by using one of O_2. H_2, N_2O, O_3, CO and CO_2 as the reaction gas while using one of Ar; He and N_2 as the carrier gas. In the gas mixture of the reaction gas to the carrier gas, the ratio of the reaction gas and the carrier gas may be 0% or more. That is, the reaction gas may or may not be used.

[0019] According to this feature, since the structure having a three-dimensional is constituted of two insulation layers comprising a surface layer of small adhesion rate and a side wall layer of large adhesion rate, and the electrode thin film can also be formed on the side wall to which it is less vapor deposited, an electrode thin film of uniform film thickness comprising Ru, RuO_2 or a mixture of Ru and RuO_2 can be prepared. Accordingly, it can provide a semiconductor device including a dielectric capacitor of a device structure having a high aspect ratio of 3 or more, corresponding to the high integration degree and having a step coverage performance. Particularly, when the structure comprising two insulation layers is MgO/SiO_2 or Al_2O_3/SiO_2, a uniform electrode thin film can be prepared depending on the different adhesion rate of the precursor.

[0020] Further, this invention has a feature in a semiconductor device having a dielectric and electrodes for applying a voltage to the dielectric in which the electrode is a thin film electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 formed on a structure with an aspect ratio of the three-dimensional structure (contact hole depth/diameter) of 3 or more.

[0021] The semiconductor device can contain an electrode thin film of a uniform thickness comprising a Ru, RuO_2 or a mixture of Ru and RuO_2 manufactured by an MOCVD process from a cyclopentadienyl complex, or an electrode thin film of a uniform thickness comprising Ru, RuO_2 or a mixture of Ru and RuO_2 manufactured by an MOCVD process from the β-diketone complex of high integration degree having a top electrode/a dielectric/a bottom electrode. Since the electrode thin film is formed homogeneously to the surface, the bottom and the side wall on the substrate having a three-dimensional, it is possible to obtain a dielectric capacitor of high integration degree and capable of functioning intactly having a three-dimensional structure of high aspect ratio. When such a dielectric capacitor is used for semiconductor devices such as DRAM, the capacity can be increased.

[0022] Further, this invention has a feature of forming the bottom electrode and the top electrode by a metalorganic chemical vapor deposition process of liquid carrying and evaporation using a starting solution in which a precursor containing a cyclopentadienyl complex is

dissolved in tetrahydrofurane, toluene, hexane or octane. According to this feature, since the precursor can be supplied stably for a long period of time, a bottom electrode and a top electrode with good film quality can be formed and a semiconductor device with high performance can be manufactured. The manufacturing method for the semiconductor device according to this invention is excellent in the mass productivity of the semiconductor device. In the manufacturing method of the semiconductor device according to this invention, a bottom electrode and a top electrode which are homogeneous and with high quality can be formed at a temperature of 180°C or higher and 250°C or lower.

[0023] Further, this invention has a feature of forming the bottom electrode and the top electrode by a metalorganic chemical vapor deposition process of liquid carrying and evaporation using a starting solution in which a precursor containing a β-diketone complex is dissolved in tetrahydrofurane, toluene, hexane or octane. According to this feature, since the precursor can be supplied stably for a long period of time, a bottom electrode and a top electrode with good film quality can be formed and a semiconductor device with high performance can be manufactured. The manufacturing method for the semiconductor device according to this invention is excellent in the mass productivity of the semiconductor device. In the manufacturing method of the semiconductor device according to this invention, a bottom electrode and a top electrode which are homogeneous and with high quality can be formed at a temperature of 300°C or higher and 500°C or lower.

[0024] When the liquid carrying and evaporation metalorganic chemical vapor deposition process using a starting solution in which a precursor containing the cyclopentadienyl complex or the β-diketone complex is dissolved in a tetrahydrofuran solvent is used, since the starting solution can be stored at a room temperature, thermal denaturation of the precursor as caused in the sublimation method can be suppressed and, as a result, the precursor can be supplied stably for a long period of time. The liquid carrying and evaporation metalorganic chemical vapor deposition process is a method of dissolving a precursor into a solvent to prepare a starting solution, heating the starting solution in an evaporator to obtain an evaporated precursor and conducting the chemical vapor deposition process.

[0025] Further, this invention has a feature in using a solvent having a solubility of 0.05 mol/l or more for the precursor such as tetrahydrofuran, toluene, hexane or octane. According to this feature, since evaporation of the precursor and the solvent is taken place simultaneously in the evaporation step of the liquid carrying and evaporation metalorganic chemical vapor deposition process, the precursor can be supplied stably for a long period of time to manufacture a semiconductor device with higher performance.

[0026] In a case of a solvent with a solubility of 0.05 mol/l or lower, only the solvent of lower boiling point is evaporated selectively in an evaporator and, as a result, the precursor of high boiling point is deposited in the inside of the evaporator to cause clogging, making it difficult to stably supply. The solubility of the diethylcyclopentadienyl ruthenium ($Ru(EtCp)_2$) complex as the cyclopentadienyl complex to each kinds of the solvents is 1.74 mol/l for tetrahydrofuran, 1.4 mol/l for toluene, 1.4 mol/l for hexane and 1.4 mol/l for octane, and the precursor can be supplied stably in the liquid carrying and evaporation metalorganic chemical vapor deposition process. Further, the solubility of the dibivaloylmethanate ruthenium ($Ru(dpm)_3$) complex as the β-diketone complex is to each kind of the solvents is 0.52 mol/l for tetrahydrofuran, 0.45 mol/l for toluene, 0.27 mol/l for hexane and 0.25 mol/l for octane and the starting material can be supplied stably in the liquid carrying and evaporation metalorganic chemical vapor deposition process.

[0027] Further, in this invention, since the organic ingredient of the precursor and the reaction gas take place combustion or reductive reaction in the course of forming the film when O_2, H_2, CO or CO_2 is used as the reaction gas, the residual carbon content in the electrode film for the bottom electrode and the top electrode can be defined to 10^{-2} at% or more and 1 at% of less, by which high quality bottom electrode and top electrode not causing contact failure can be formed and a semiconductor device with high performance can be manufactured.

[0028] Further, this invention has a feature in a method of forming a thin film to the surface and the lateral side of a structure having a three-dimensional in which the structure comprises in lamination a two layered structure of a surface layer with small adhesion rate and a side wall layer with a large adhesion rate for the starting thin film material. Use of the 2-layered structure explained in Fig. 3 is not restricted only to the case of forming the Ru thin film as the electrode by the MOCVD process and is generally applicable also in the film forming method such as a sputtering method, a vacuum vapor deposition method or an MBE method as a method for forming a homogeneous film to the surface, the side wall and the bottom in a case where the film tends to be deposited preferentially only to the surface.

Brief Description of Drawings

[0029]

Fig. 1 shows cross sectional SEM images for an Ru film obtained at O_2/Ar ratio of 5% in this invention.

Fig. 2 is a crystal structural view of a β-diketone complex.

Fig. 3 is a cross sectional view illustrating a structure comprising a two layered insulation layer.

Fig. 4 is a cross sectional view of an example of a dielectric capacitor contained in a semiconductor device manufactured according to this invention.

Fig. 5 is a crystal structural view of a cyclopentadienyl complex.

Fig. 6 is a cross sectional view of another example of a dielectric capacitor contained in a semiconductor device manufactured according to this invention.

Fig. 7 is a cross sectional view of a further example of a dielectric capacitor contained in a semiconductor device manufactured according to this invention.

Fig. 8 is a cross sectional view of a DRAM cell manufactured according to this invention.

Best Mode for Carrying Out the Invention

[0030] A method of manufacturing a semiconductor device according to this invention is to be explained specifically with reference to the drawings.

[Example 1]

[0031] A method of manufacturing a semiconductor device using a crystal structure shown in Fig. 5 of a discyclopentadienyl ruthenium ($RuCp_2$) complex in which R = H is shown below. Fig. 4 is a cross sectional view of a dielectric capacitor contained in a semiconductor device manufactured in this example.

[0032] At first, an Si wafer 41 was heated to 300°C and a contact hole is opened in an SiO_2 layer 44 formed by thermal oxidation and then an Si plug 42 is prepared. Then, a barrier layer 43 made of a TiN layer of 100 Å thickness was prepared on the Si plug 42 by a sputtering method. Further, after forming an SiO_2 layer 45 of 8000 Å thickness by a plasma CVD process using starting TEOS material, a 2400 Å diameter was fabricated around the contact hole as a center to prepare a substrate having a three-dimensional. The aspect ratio (contact hole depth/diameter) of the three-dimensional structure is 3.33.

[0033] A bottom electrode 46 was prepared on the substrate. For the preparation of the bottom electrode 46, an $RuCp_2$ complex was formulated at a concentration of 0.05 to 0.25 mol/l into a THF (tetrahydrofuran) solvent to form a CVD precursor. The CVD precursor was supplied at a rate of 0.1 to 3 sccm by using a liquid mass flow controller. After converting the CVD precursor all at once from liquid to gas by setting the temperature of a vaporizer to 80 to 150°C, it was carried on an Ar gas at 198 to 500 sccm. Then, after mixing the CVD/Ar gas with oxygen gas at 2 to 800 sccm, they were introduced into a reactor. The pressure in the reactor was set to 0.01 to 50 torr, the film forming temperature was set to 180°C or higher and 250°C or lower to form film for 1 to 20 min to obtain a film thickness of 20 to 30 nm.

[0034] As a result of measurement by X-ray diffractiometry for the obtained film, it was found to be an Ru film at 1 to 25%, an Ru/RuO_2 mixed film at 25 to 50% and an RuO_2 film at 50 to 400%. Further, the film is in the form of RuO_2 even if the O_2/Ar ratio is 400% or more. By the way, in a case where O_2/Ar = 0%, granular crystals were formed to provide inhomogeneous film quality.

[0035] Fig. 1 shows cross sectional SEM images of the Ru film obtained at the O_2/Ar ratio of 5%. It was found that the Ru film was formed homogeneously to the surface, the bottom and the side wall and the film has a step coverage (film side wall/film surface) of 100%. Further, the surface roughness of the film was ±10 Å or less and the film quality was extremely smooth. As a result of measurement for the specific resistivity, the resistance was as low as $\rho = 50\ \mu\Omega/cm^2$ at a room temperature.

[0036] Further, when the residual amount of carbon was analyzed along the direction of the depth in the film by secondary ion mass spectroscopy, the carbon content was within a range from 10^{-2} at% or more to 1 at% or less and it was a thin film with high quality.

[0037] Then, (Ba, Sr)TiO_3(BST) was prepared as a dielectric 47 on the bottom electrode 46 by an MOCVD process. Barium dibivaloylmethanate $Ba(dpm)_2$, Sr $(dpm)_2$ and $Ti(O\text{-}i\text{-}Pr)_2(dpm)_2$ were used for the precursors and each of the materials was prepared at a concentration of 0.05 to 0.25 mol/l into a THF solvent to form a CVD precursor. Each of the CVD precursor was supplied at a rate of 0.1 to 3 sccm from a liquid mass flow controller to an evaporator set to 250°C. The CVD precursor gas was introduced by the Ar carrier gas at 200 sccm into the reactor and 5 to 100 sccm of an oxygen gas was also introduced to the reactor. Film adhesion was conducted for 3 min by setting the pressure of the reactor to 0.01 to 50 torr and a film forming temperature to 420°C, to form a BST thin film to 30 nm.

[0038] Then, the film was heat treated at 700°C for 30 to 60 sec in an N_2 or Ar gas to improve the crystallinity. A top electrode 48 was formed on the dielectric 47. The film was formed by the same method and under the same conditions as those for forming the bottom electrode 46, to obtain a homogeneous thin Ru film with 100% step coverage on the three-dimensional with an aspect ratio of 6.17. The thus obtained dielectric capacitor showed excellent electrical characteristics with the specific dielectric constant ε at 1 V of 300.

[0039] In addition to the discyclopentadienyl ruthenium complex in which R = H, homogeneous thin Ru films could be formed as the bottom electrode and the top electrode by the same method as described above also in a case of using dis(methylcyclopentadienyl) ruthenium at R = CH_3, dis(ethylcyclopentadienyl) ruthenium at R = C_2H_5, dis(propylcyclopentadienyl) ruthenium at R = C_3H_7, dis(butylclopentadienyl) ruthenium at R = C_4H_9.

[0040] Further, while O_2 was used as the reaction gas as described above, a homogeneous thin Ru film could be formed also by using one of H_2, N_2O, O_3, CO and CO_2. Further, while the Ar gas has been explained as the carrier gas, an He or N_2 gas may also be used and it has been found that any combination of them can form an Ru film at 1 to 25%, an Ru/RuO_2 mixed film at 25 to 50% and an RuO_2 film at 50 to 400% or more as the

reaction gas to the carrier gas ratio.

[Example 2]

[0041] A method of manufacturing a semiconductor device using a crystal structure of β-diketone complex shown in Fig. 2 of a dibivaloylmethanate ruthenium (Ru $(dpm)_3$) complex in which R' = $C(CH_3)_3$ is shown below. Fig. 6 is a cross sectional view of a dielectric capacitor contained in a semiconductor device manufactured in this example.

[0042] In the same manner as in Example 1, after opening a contact hole to an SiO_2 layer 64 formed by thermally oxidizing an Si wafer 61, preparing an Si plug 62 and then forming a TiN barrier layer 63, an insulation layer 65 of an SiO_2 layer was prepared to a thickness of 7800 Å by a plasma CVD process. Then, an MgO layer was deposited as an insulation layer 66 by a sputtering process using Mg as a target. A film of 200 Å thickness was obtained by using a 1:1 gas mixture of oxygen and argon as a sputtering gas at a film forming pressure of 2 Pa and with RF power of 200 W. A 2400 Å diameter was fabricated around a contact hole as a center to prepare a substrate having a three-dimensional structure. The aspect ratio of the three-dimensional structure is 3.33.

[0043] A bottom electrode 67 was prepared on the substrate. For the preparation of the bottom electrode 67, dibivaloylmethanate ruthenium ($Ru(dpm)_3$) of the crystal structure of the β-diketone complex at R' = $C(CH_3)_3$ shown in Fig. 2 was formulated at a concentration of 0.05 to 0.25 mol/l in a THF solvent to form a CVD precursor. The CVD precursor was supplied at a rate of 0.1 to 3 sccm by using a liquid mass flow controller. After converting the CVD precursor all at once from liquid to gas by setting the temperature for the evaporator to 100 to 200°C, it was carried on an Ar gas at 198 to 500 sccm. Then, after mixing the CVD/Ar gas and an oxygen gas at 0 to 800 sccm, they were introduced into a reactor. A film of 20 to 30 nm thickness was obtained by depositing a film at a pressure of the reactor of 0.01 to 50 torr, at a film forming temperature of 300°C or higher to 500°C or lower for 1 to 20 min.

[0044] As a result of measurement by X-ray diffractiometry for the obtained film, it has been found that the film is an Ru film at 0 to 25% or less, an Ru/RuO_2 mixed film at 25 to 50% or less and an RuO_2 film at 50 to 400% or more as O_2/Ar ratio. From the result of SEM observation for the cross section of the Ru film of 20 nm thickness obtained at the O_2/Ar ratio of 0%, it has been found that the Ru film was formed homogeneously to the surface, the bottom and the side wall and the step coverage of the film (film side wall/film surface) was about 100%. Further, the surface roughness of the film was ±8 Å or less showing extremely smooth film quality. As a result of measurement for the specific resistivity, the resistance was as low as ρ = 50 μΩ/cm² at a room temperature.

[0045] Then, BST was prepared to a film thickness of 30 nm as a dielectric 68 on the bottom electrode 67 by an MOCVD process in the same manner as in Example 1. Then, a heat treatment was applied in an N_2 or Ar gas at 700°C for 30 to 60 sec, to improve the crystallinity. A top electrode 69 was formed on the dielectric 68. The top electrode 69 was formed by forming a film by the same method and under the same conditions as those in the formation of the bottom electrode 67 and a homogeneous thin Ru film with 100% step coverage could be formed on the aspect ratio of 6.17. The thus obtained dielectric capacitor showed excellent electrical characteristics with the specific dielectric constant ε of 300 at 1 V.

[0046] An identical homogeneous thin Ru film could also be prepared by using an Al_2O_3 layer manufactured by a sputtering process using Al as a target instead of MgO as an insulation layer 66.

[0047] Homogeneous Ru thin films could be formed on the bottom electrode and the top electrode by the same method as described above also in a case of using acetylacetonate ruthenium at R = CH_3 and hexafluoroacetyl acetonate ruthenium at R = CF_3 in addition to the dibivaloylmethanate ruthenium complex at R = $C(CH_3)_3$.

[0048] Further, while O_2 was used as the reaction gas, a homogeneous Ru thin film could be formed also by using one of H_2, N_2O, O_3, CO and CO_2. Further, while description has been made to the Ar gas as the carrier gas, an He or N_2 gas may also be used and it has been found that any combination of them could form an Ru film at a ratio of 0 to 25%, an Ru/RuO_2 mixed film at 25 to 50% and an RuO_2 film at 50 to 400% or more as the reaction gas to the carrier gas ratio.

[Example 3]

[0049] A third example of this invention is to be explained with reference to Fig. 7. Fig. 7 is a cross sectional view of a dielectric capacitor contained in a semiconductor device manufactured in this example.

[0050] In the same manner as in Example 1, after opening a contact hole to an SiO_2 layer 74 formed by thermally oxidizing an Si wafer 71, preparing an Si plug 72 and then forming a TiN barrier layer 73, an Ru layer was formed by a sputtering process using Ru as a target. A film of 5000 Å thickness was obtained by using an Ar gas as a sputtering gas, at a film forming pressure of 2 Pa and with an RF power of 1200 W. Then, a top electrode 75 having a three-dimensional was formed by fabricating a trapezoidal shape around the contact hole as a center. The aspect ratio of the three-dimensional structure is 3.0.

[0051] Then, BST as a dielectric 76 was formed to 30 nm film thickness on the bottom electrode 75 by an MOCVD process in the same method as in Example 1. Then, a heat treatment was applied in an N_2 or Ar gas at 700°C for 30 to 60 sec to improve the crystallinity. A top electrode 77 was formed on the dielectric 76. The

top electrode 77 was formed by preparing a thin film of Ru, RuO_2 or a mixture of Ru and RuO_2 at a thickness of 20 nm under the same conditions as those in Example 1 by a CVD process using $RuCp_2$/THF precursor. The resultant dielectric capacitor showed excellent electrical characteristics with a specific dielectric constant ε of 1 V at 280.

[Example 4]

[0052] A fourth example of this invention is to be explained with reference to Fig. 8. Fig. 8 is a cross sectional view of DRAM as a semiconductor device using the dielectric capacitor prepared in Example 1.

[0053] Device isolation oxide films 83a, 83b were prepared by an oxidizing method on a P-type semiconductor substrate 81, and N-type source/drain regions 80a, 80b, 80c were prepared on the main surface of the semiconductor substrate by ion implantation. Gate electrodes 81a, 82b, 82c and 82d each of 200 nm film thickness were formed by way of a gate oxide film of 12 nm thickness on a channel region. A buried bit line 84 connected electrically was formed on the source/drain region 80b by photolithography and dry etching, and an SiO_2 layer 14 was formed so as to cover the entire surface. Subsequently, a dielectric capacitor comprising a top electrode, a dielectric and a bottom electrode was prepared by the method shown in Example 1. Then, after forming an interlayer insulation film 88 so as to cover the top electrode 19, the film was flattened by a chemical etching method. First layer aluminum wirings were formed at a space thereon, an insulation protective film 86 was prepared so as to cover the wirings and a second layer aluminum wiring layers 87 were formed thereon. In the same manner as described above, DRAM can be prepared also by using the dielectric capacitor prepared in Example 2.

[0054] While the THF solvent was used in the MOCVD process for forming the top electrode and the bottom electrode in Examples 1 to 4, there is no particular restriction for the solvent so long as it is a material capable of dissolving the precursor and toluene or ether may be used, for example, with no troubles.

[0055] Furthermore, the method of forming the top electrode and the bottom electrode explained in Examples 1 to 4 is the MOCVD process starting from a starting precursor but similar effects could also be obtained by a material gas supply method by a sublimation method from a solid precursor or a starting gas supply method by a bubbling method from a liquid precursor. Particularly, since the precursor can be supplied stably for a long period of time by forming the bottom electrode and the top electrode by a liquid carrying and evaporation metalorganic chemical vapor deposition method, the bottom electrode and the top electrode with good film quality can be formed to manufacture a semiconductor device with high performance.

Industrial Applicability

[0056] According to this invention, a semiconductor device containing a dielectric capacitor having an excellent step coverage for a device structure of a high aspect ratio corresponding to high degree of integration can be obtained.

Claims

1. A method of manufacturing a semiconductor device of laminating to form a bottom electrode, a dielectric and a top electrode on an underlying substrate having a three-dimensional structure in which
   the bottom electrode and the top electrode are formed by an metalorganic chemical vapor deposition process at 180°C or higher and 250°C or lower using a cyclopentadienyl complex as a precursor.

2. A method of manufacturing a semiconductor device as defined in claim 1, wherein one of O_2, H_2, N_2O, O_3, CO and CO_2 is used as a reaction gas and the ratio of the reaction gas to a carrier gas is 1% or more.

3. A method of manufacturing a semiconductor device of laminating to form a bottom electrode, a dielectric and a top electrode on an substrate having a three-dimensional structure in which
   the structure having a three-dimensional is constituted of an insulation layer of a 2-layered structure comprising a surface layer with a smaller adhesion rate and a side wall layer with a larger adhesion rate for an electrode precursor, and the bottom electrode and the top electrode are formed by a metalorganic chemical vapor deposition process at 300°C or higher and 500°C or lower using a β-diketone complex as the precursor.

4. A method of manufacturing a semiconductor device as defined in claim 3, wherein the structure constituted of the 2-layered insulation layer comprises MgO/SiO_2 or Al_2O_3/SiO_2.

5. A method of manufacturing a semiconductor device as defined in any one of claims 1 to 4, wherein each of the top electrode and the bottom electrode comprises Ru, RuO_2 or a mixture of Ru and RuO_2.

6. A semiconductor device having a dielectric and an electrode applying a voltage to the dielectric in which the electrode is a thin film electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 formed on a structure with an aspect ratio of a three-dimensional structure (contact hole depth/diameter) of 3 or more.

7. A method of forming a thin film to the surface and the lateral side of structure having a three-dimensional, in which the structure is constituted of a 2-layered structure formed by laminating a surface layer with a smaller adhesion rate and a side wall layer with a larger adhesion rate of a starting thin film material.

8. A method of manufacturing a semiconductor device of laminating to form a bottom electrode, a dielectric and a top electrode on a substrate having a three-dimensional structure in which,

the bottom electrode and the top electrode are formed by using a starting precursor in which a starting metalorganic material containing a cyclopentadienyl complex is dissolved in tetrahydrofuran, toluene, hexane or octane, by a liquid carrying and evaporation, metalorganic chemical vapor deposition process.

9. A method of manufacturing a semiconductor device as defined in claim 8, wherein the bottom electrode and the top electrode are formed at 180°C or higher and 250°C or lower.

10. A method of manufacturing a semiconductor device of laminating to form a bottom electrode, a dielectric and a top electrode on substrate having a three-dimensional structive in which,

the bottom electrode and the top electrode are formed by using a starting precursor in which a starting metalorganic material containing a β-diketone complex is dissolved in tetrahydrofuran, toluene, hexane or octane, by a liquid carrying and evaporation, metalorganic chemical vapor deposition process.

11. A method of manufacturing a dielectric capacitor as defined in claim 10, wherein the bottom electrode and the top electrode are formed at 300°C or higher and 500°C or lower.

12. A method of manufacturing a semiconductor device as defined in claim 8 or 10, wherein the tetrahydrofuran, the toluene, the hexane or the octane is a solvent having a solubility for the starting precursor of 0.05 mol/l or more.

13. A semiconductor device formed by laminating a bottom electrode, a dielectric and a top electrode in which the oxygen content of the bottom electrode and the top electrode is 10^{-2} at% or more and 1 at% or less.

14. A semiconductor device manufactured in accordance with the manufacturing method as defined in claim 1, 3, 6, 7 or 10.

1. A method of manufacturing a semiconductor device by laminating to form a bottom electrode (46; 67; 75), a dielectric (47; 68; 76) and a top electrode (48; 69; 77) on an underlying substrate (41-45; 61-65; 71-75) having a three-dimensional structure in which

the bottom electrode (46; 67; 75) and the top electrode (48; 69; 77) are formed by a metalorganic chemical vapor deposition process at 180°C or higher and 250°C or lower using a cyclopentadienyl complex as a precursor.

2. A method of manufacturing a semiconductor device as defined in claim 1, wherein one of O_2, H_2, N_2O, O_3, CO and CO_2 is used as a reaction gas and the ratio of the reaction gas to a carrier gas is 1% or more.

3. A method of manufacturing a semiconductor device by laminating to form a bottom electrode (46; 67; 75), a dielectric (47; 68; 76) and a top electrode (48; 69; 77) on an substrate (41-45; 61-65; 71-75) having a three-dimensional structure in which

the three-dimensional structure is constituted of an insulation layer of a 2-layered structure comprising a surface layer with a smaller adhesion rate and a side wall layer with a larger adhesion rate for an electrode precursor, and the bottom electrode and the top electrode are formed by a metalorganic chemical vapor deposition process at 300°C or higher and 500°C or lower using a β-diketone complex as the precursor.

4. A method of manufacturing a semiconductor device as defined in claim 3, wherein the structure constituted of the 2-layered insulation layer comprises MgO/SiO_2 or Al_2O_3/SiO_2.

5. A method of manufacturing a semiconductor device as defined in any one of claims 1 to 4, wherein each of the top electrode (48; 69; 77) and the bottom electrode (46; 67; 75) comprises Ru, RuO_2 or a mixture of Ru and RuO_2.

6. A semiconductor device having a dielectric and an electrode (46, 48; 67, 69; 75, 77) applying a voltage to the dielectric (46; 68; 76) in which the electrode is a thin film electrode comprising Ru, RuO_2 or a mixture of Ru and RuO_2 formed on a structure (41-45; 61-65; 71-75) with an aspect ratio of a three-dimensional structure (contact hole depth/diameter) of 3 or more.

7. A method of forming a thin film to the surface and the lateral side of a three-dimensional structure (41-45; 61-65; 71-75), in which the structure is constituted of a 2-layered structure formed by laminating a surface layer with a smaller adhesion rate and

a side wall layer with a larger adhesion rate of a starting thin film material.

8. A method of manufacturing a semiconductor device by laminating to form a bottom electrode (46; 67; 75), a dielectric (47; 68; 76) and a top electrode (48; 69; 77) on a substrate (41-45; 61-65; 71-75) having a three-dimensional structure in which,

the bottom electrode and the top electrode are formed by using a starting precursor in which a starting metalorganic material containing a cyclopentadienyl complex is dissolved in tetrahydrofuran, toluene, hexane or octane, by a liquid carrying and evaporation, metalorganic chemical vapor deposition process.

9. A method of manufacturing a semiconductor device as defined in claim 8, wherein the bottom electrode and the top electrode are formed at 180°C or higher and 250°C or lower.

10. A method of manufacturing a semiconductor device by laminating to form a bottom electrode (46; 67; 75), a dielectric (47; 68; 76) and a top electrode (48; 69; 77) on substrate (41-45; 61-65; 71-75) having a three-dimensional structive in which:

the bottom electrode and the top electrode are formed by using a starting precursor in which a starting metalorganic material containing a β-diketone complex is dissolved in tetrahydrofuran, toluene, hexane or octane, by a liquid carrying and evaporation, metalorganic chemical vapor deposition process.

11. A method of manufacturing a dielectric capacitor as defined in claim 10, wherein the bottom electrode and the top electrode are formed at 300°C or higher and 500°C or lower.

12. A method of manufacturing a semiconductor device as defined in claim 8 or 10, wherein the tetrahydrofuran, the toluene, the hexane or the octane is a solvent having a solubility for the starting precursor of 0.05 mol/l or more.

13. A semiconductor device formed by laminating a bottom electrode (46; 67; 75), a dielectric (47; 68; 76) and a top electrode (48; 69; 77) in which the oxygen content of the bottom electrode and the top electrode is 10^{-2} at% or more and 1 at% or less.

14. A semiconductor device manufactured in accordance with the manufacturing method as defined in claim 1, 3, 6, 7, 8 or 10.

FIG. 1

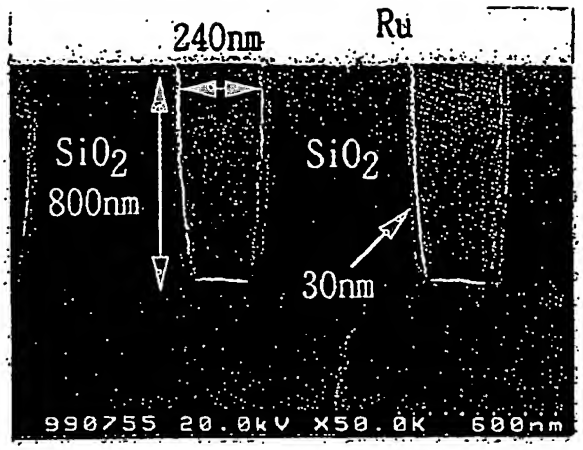
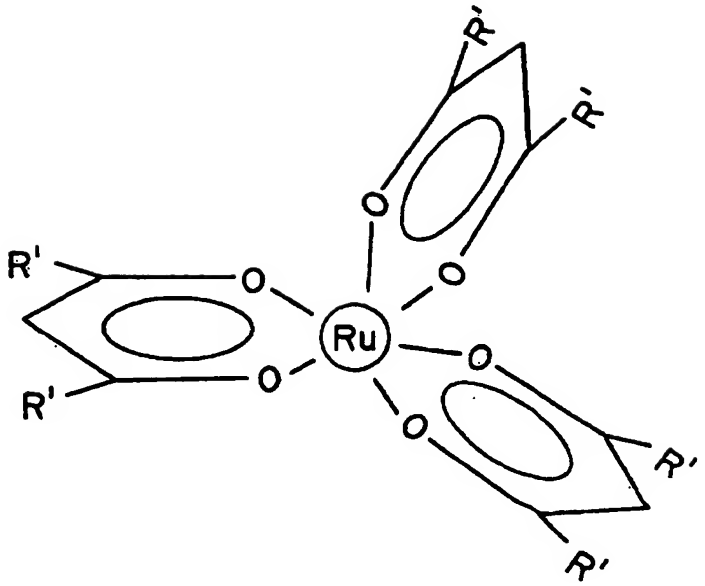


FIG. 2



R= $C(CH_3)_3$, CH_3, CF_3

FIG. 3

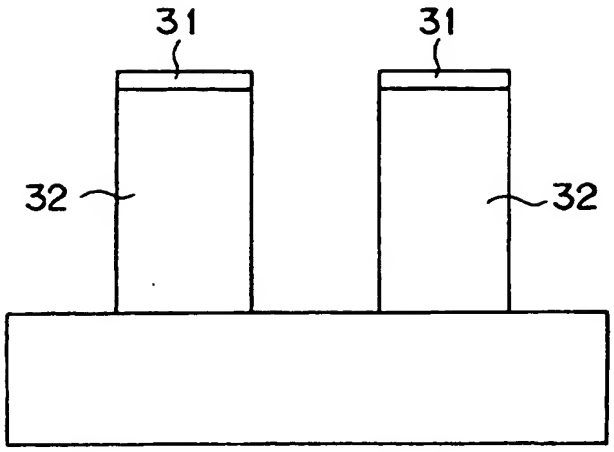


FIG. 4

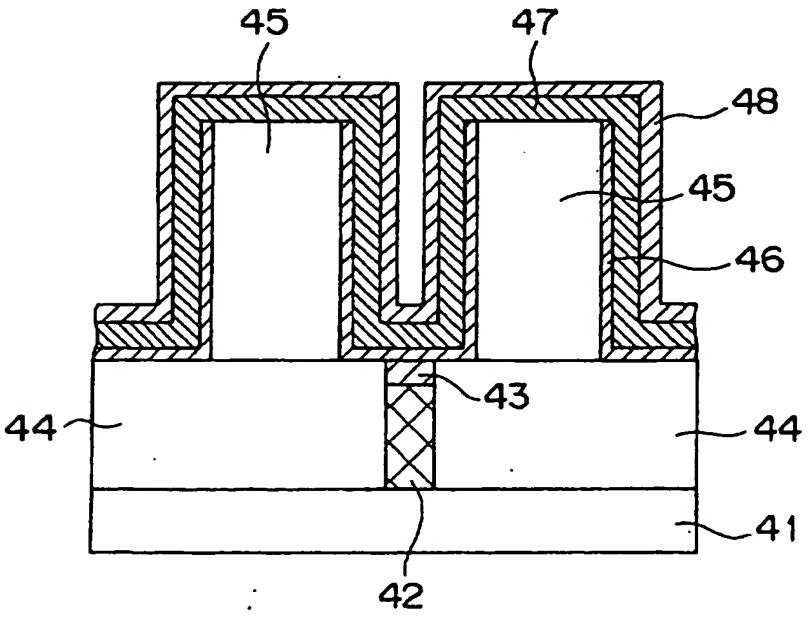
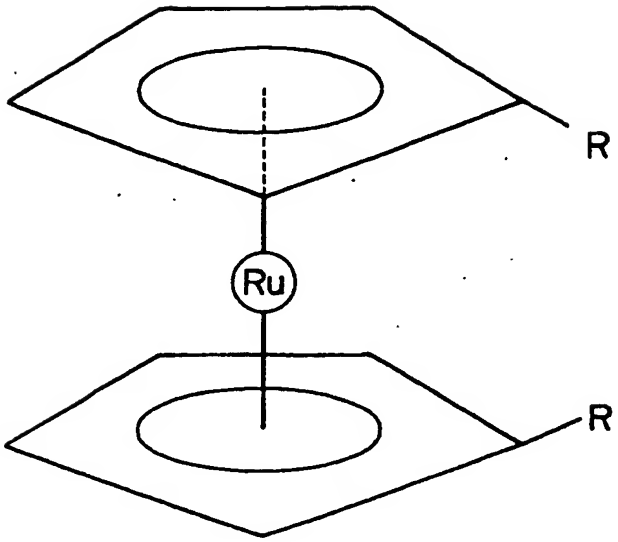


FIG. 5



R=H, CH_3, C_2H_5, C_3H_7 AND C_4H_9

FIG. 6

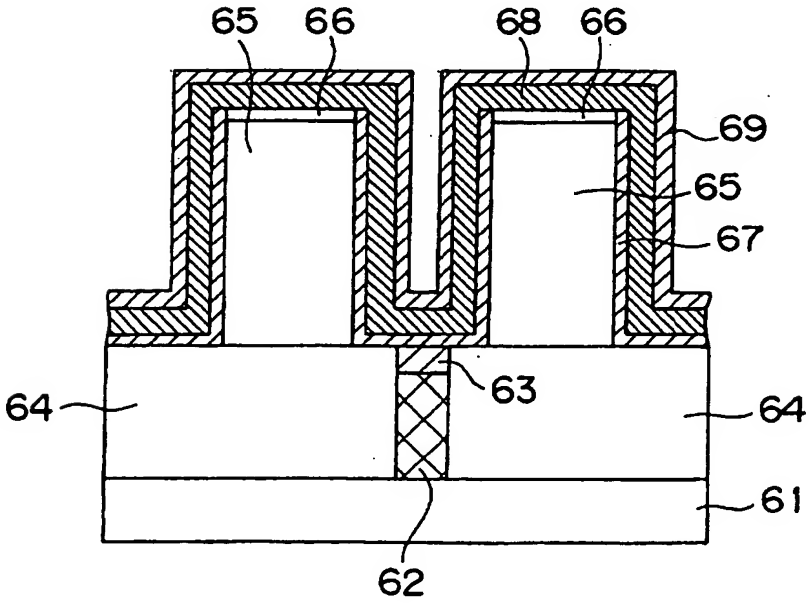


FIG. 7

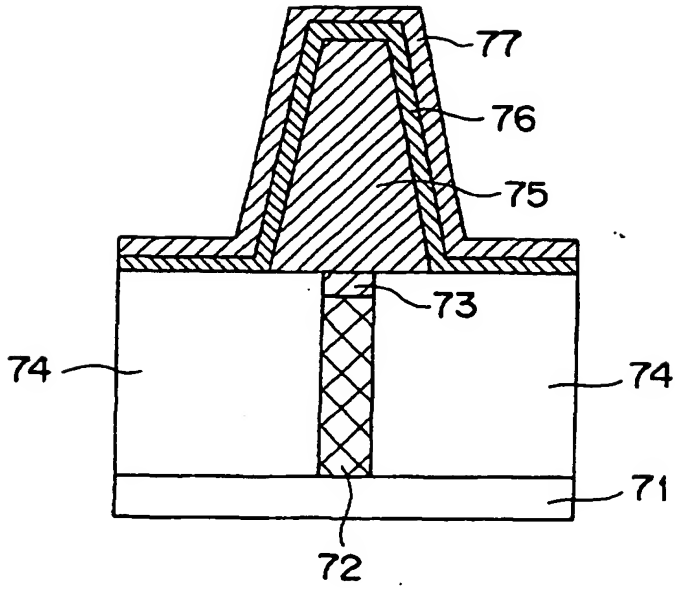
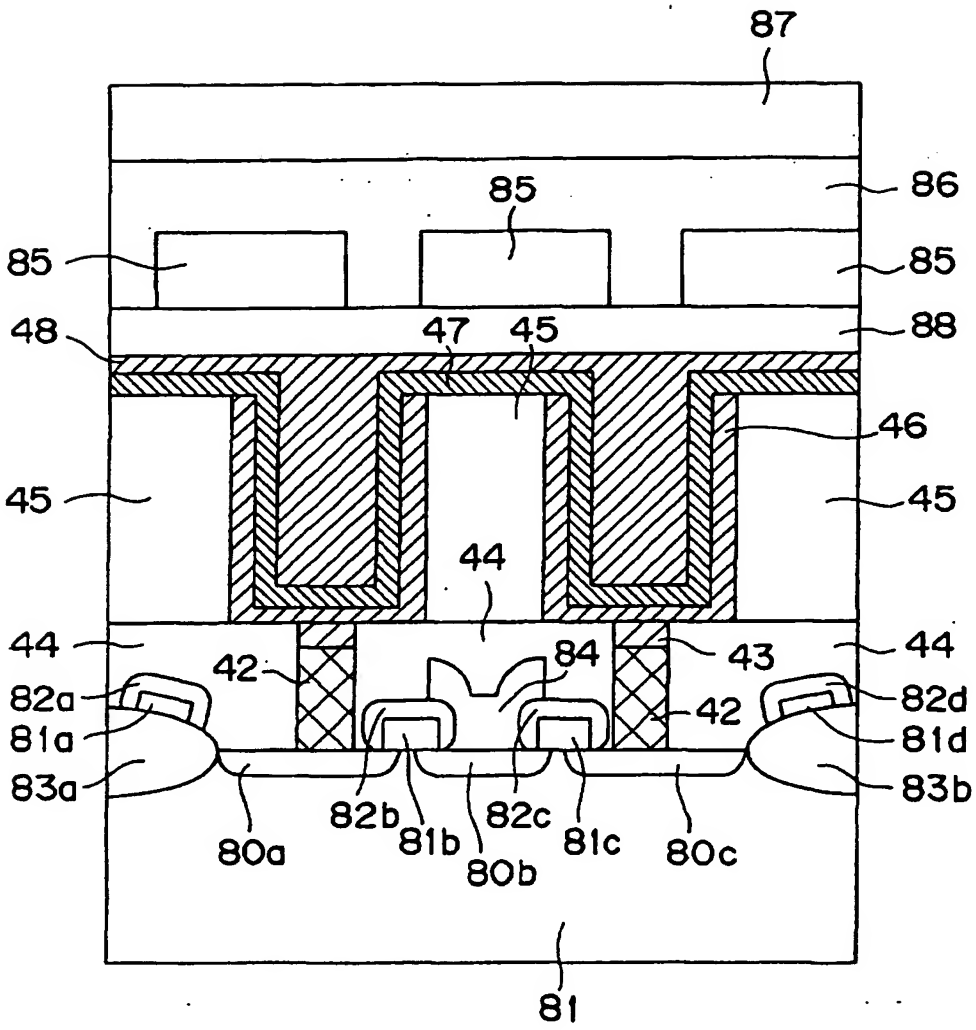


FIG. 8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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/05574

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L21/28
H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L21/28
H01L21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1999 Toroku Jitsuyo Shinan Koho 1994-1999
Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US, 5130172, A (The Regents of the University of California, Berkeley, Calif.), 14 July, 1992 (14.07.92), Claim 1,6 (Family: none)	1,2,5,14 8,9,12 3,4,6,7,10, 11,13
Y	JP, 9-246214, A (Fujitsu Limited), 19 September, 1997 (19.09.97), Par. Nos. [0002]-[0005] & US, 5874364, A (23.02.99)	1-13
EY EA	JP, 11-35589 (Kojundo Chem. Lab. Co., Ltd.), 09 February, 1999 (09.02.99), Par. Nos. [0027]-[0028] (Family: none)	1,2,5,8,9,12, 14 3,4,6,7,10, 11,13
Y A	JP, 9-49081 (DOWA MINING CO., LTD.), 18 February, 1997 (18.02.97), Par. Nos. [0017]-[0020] (Family: none)	3,4,5,10-12,14 1,2,6-9,13
Y A	JP, 6-283438 (NIPPON SANSO CORPORATION), 07 October, 1994 (07.10.94), Par. Nos. [0009]-[0011] (Family: none)	3,4,5,10-12,14 1,2,6-9,13

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 December, 1999 (28.12.99)	11 January, 2000 (11.01.00)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/05574

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 10-163131 (Fujitsu Limited), 19 June, 1998 (19.06.98), Par. No. [0011] (Family: none)	1-14
Y	JP, 10-195656 (Matsushita Electric Ind. Co., Ltd.), 28 July, 1998 (28.07.98), Claims 1, 2; par. Nos. [0009]-[0011] (Family: none)	1-14
A	JP, 9-36062 (MITSUBISHI MATERIALS CORPORATION), 07 February, 1997 (07.02.97), Par. No. [0027] (Family: none)	8,10

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